National Semiconductor

January 2001

CLC5602
Dual, High Output, Video Amplifier

General Description

The National CLC5602 has a new output stage that delivers high output drive current (130mA), but consumes minimal quiescent supply current (1.5mA/ch) from a single 5V supply. Its current feedback architecture, fabricated in an advanced complementary bipolar process, maintains consistent performance over a wide range of gains and signal levels, and has a linear phase response up to one half of the −3dB frequency.

The CLC5602 offers a 0.1dB gain flatness to 22MHz and differential gain and phase errors of 0.06
and 0.02%. These features are ideal for professional and consumer video applications.

The CLC5602 offers superior dynamic performance with a 135MHz small-signal bandwidth, 300V/µs slew rate and a 5.7ns rise/fall times ($2V_{STEP}$). The combination of low quiescent power, high output current drive, and high speed performance make the CLC5602 well suited for many battery powered personal communication/computing systems.

The ability to drive low impedance, highly capacitive loads, makes the CLC5602 ideal for single ended cable applications. It also drives low impedance loads with minimum distortion. The CLC5602 will drive a 100Ω load with only −86/−85dBc second/third harmonic distortion (A_V = +2, V_{OUT} = $2V_{PP}$, f = 1MHz). With a 25Ω load, and the same conditions, it produces only −86/−72dBc second/third harmonic distortion.

The CLC5602 can also be used for driving differential-input step-up transformers for applications such as Asynchronous Digital Subscriber Lines (ADSL) or High-Bit-Rate Digital Subscriber Lines (HDSL).

When driving the input of high resolution A/D converters, the CLC5602 provides excellent −87/−95dBc second/third harmonic distortion (A_V =+ 2, V_{OUT} =2 V_{PP}, f =1 MHz, R_L = 1kΩ) and fast settling time.

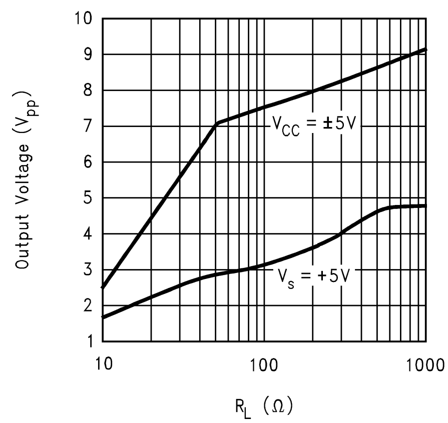
Features

- 130mA output current
- 0.06%, 0.02° differential gain, phase
- 1.5mA/ch supply current
- 135MHz bandwidth (A_v=+2)
- −87/−95dBc HD2/HD3 (1MHz)
- 15ns settling to 0.05%
- 300V/µs slew rate
- Stable for capacitive loads up to 1000pf
- Single 5V or ±5V supplies

Applications

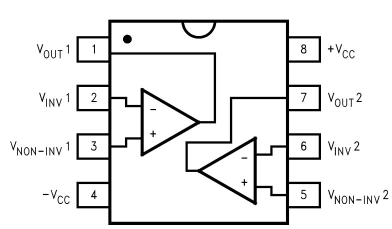
- Video line driver
- ADSL/HDSL driver
- Coaxial cable driver
- UTP differential line driver
- Transformer/coil driver
- High capacitive load driver
- Portable/battery powered applications
- Differential A/D driver

Maximum Output Voltage vs. R_L



DS015000-1

Connection Diagram



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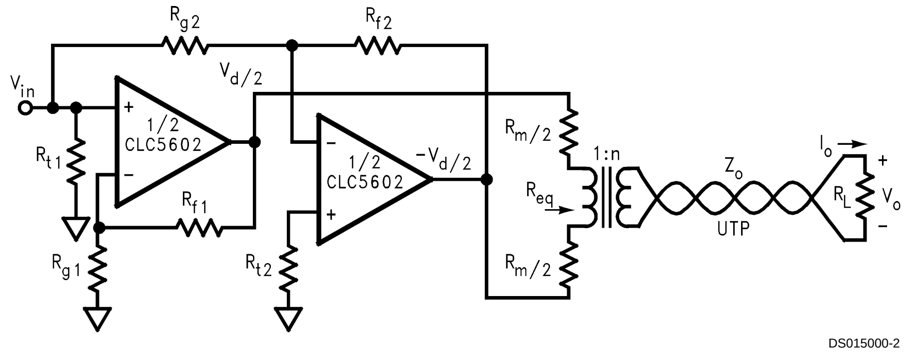
Pinout
DIP & SOIC

Typical Application



Recommended Inverting Gain Configuration

Ordering Information

Package	Temperature Range Industrial	Part Number	Package Marking	NSC Drawing
8-pin plastic DIP	−40˚C to +85˚C	CLC5602IN	CLC5602IN	N08E
8-pin plastic SOIC	−40˚C to +85˚C	CLC5602IM	CLC5602IM	M08A
		CLC5602IMX	CLC5602IM	

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC}-V_{EE})	+14V
Output Current (Note 4)	140mA
Common-Mode Input Voltage	V_{EE} to V_{CC}
Maximum Junction Temperature	+150˚C
Storage Temperature Range	−65˚C to +150˚C
Lead Temperature (soldering 10 sec)	+300˚C
ESD (human body model)	1000V

Operating Ratings

Thermal Resistance

Package	(θ_{JC})	(θ_{JA})
MDIP	65˚C/W	130˚C/W
SOIC	50˚C/W	145˚C/W

+5V Electrical Characteristics

(A_V = +2, R_f = 750Ω, R_L = 100Ω, V_S = +5V(Note 5), V_{CM} = V_{EE} + (V_S/2), R_L tied to V_{CM}; unless specified

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
Ambient Temperature		CLC5602IN/IM	+25˚C	+25˚C	0 to 70˚C	−40 to 85˚C	
Frequency Domain Response							
	-3dB Bandwidth	V_O = 0.5V_{PP}	100	85	75	70	MHz
		V_O = 2.0V_{PP}	65	60	55	50	MHz
	−0.1dB Bandwidth	V_O = 0.5V_{PP}	22	20	17	15	MHz
	Gain Peaking	<200MHz, V_O = 0.5V_{PP}	0	0.5	0.9	1.0	dB
	Gain Rolloff	<30MHz, V_O = 0.5V_{PP}	0.1	0.3	0.4	0.5	dB
	Linear Phase Deviation	<30MHz, V_O = 0.5V_{PP}	0.3	0.5	0.6	0.6	deg
	Differential Gain	NTSC, R_L = 150Ω to −1V	0.04	–	–	–	%
	Differential Phase	NTSC, R_L = 150Ω to −1V	0.09	–	–	–	deg
Time Domain Response							
	Rise and Fall Time	2V Step	6.1	8.5	9.2	10.0	ns
	Settling Time to 0.05%	1V Step	25	35	50	80	ns
	Overshoot	2V Step	10	20	22	22	%
	Slew Rate	2V Step	220	190	165	150	V/µs
Distortion And Noise Response							
	2nd Harmonic Distortion	2V_{PP},1MHz	−77	−74	−71	−71	dBc
		2V_{PP}, 1MHz; R_L = 1KΩ	−80	−77	−75	−70	dBc
		2V_{PP}, 5MHz	−63	−59	−57	−57	dBc
	3rd Harmonic Distortion	2V_{PP},1MHz	−85	−81	−78	−78	dBc
		2V_{PP},1MHz; R_L=1KΩ	−82	−79	−76	−76	dBc
		2V_{PP}, 5MHz	−62	−57	−54	−54	dBc
	Equivalent Input Noise						
	Voltage (e_{ni})	>1MHz	3.4	4.4	4.9	4.9	nV/$\sqrt{Hz}$
	Non-Inverting Current (i_{bn})	>1MHz	6.3	8.2	9.0	9.0	pA/$\sqrt{Hz}$
	Inverting Current (i_{bi})	>1MHz	8.7	11.3	12.4	12.4	pA/$\sqrt{Hz}$
	Crosstalk (Input Referred)	10MHz, 1V_{PP}	−72	–	–	–	dB
Static, DC Performance							
	Input Offset Voltage (Note 3)		1	4	5	6	mV
	Average Drift		7	–	15	15	µV/˚C
	Input Bias Current (Non-Inverting) (Note 3)		5	12	15	16	µA
	Average Drift		25	–	60	60	nA/˚C
	Input Bias Current (Inverting) (Note 3)		3	10	12	13	µA
	Average Drift		10	–	20	20	nA/˚C

+5V Electrical Characteristics (Continued)

(A_V = +2, R_f = 750Ω, R_L = 100Ω, V_S = +5V(Note 5), V_{CM} = V_{EE} + (V_S/2), R_L tied to V_{CM}; unless specified

Symbol	**Parameter**	**Conditions**	**Typ**	**Min/Max Ratings** (Note 2)			**Units**
Static, DC Performance							
	Power Supply Rejection Ratio	DC	48	45	43	43	dB
	Common Mode Rejection Ratio	DC	49	47	45	45	dB
	Supply Current Per Channel (Note 3)	R_L = ∞	1.5	1.7	1.8	1.8	mA
Miscellaneous Performance							
	Input Resistance (Non-Inverting)		0.46	0.36	0.32	0.32	MΩ
	Input Capacitance (Non-Inverting)		1.8	2.75	2.75	2.75	pF
	Input Voltage Range, High		4.2	4.1	4.1	4.0	V
	Input Voltage Range, Low		0.8	0.9	0.9	1.0	V
	Output Voltage Range, High	R_L = 100Ω	4.0	3.9	3.9	3.8	V
	Output Voltage Fange, Low	R_L = 100Ω	1.0	1.1	1.1	1.2	V
	Output Voltage Range, High	R_L = ∞	4.1	4.0	4.0	3.9	V
	Output Voltage Range, Low	R_L = ∞	0.9	1.0	1.0	1.1	V
	Output Current (Note 4)		100	80	65	40	mA
	Output Resistance, Closed Loop	DC	55	90	90	120	mΩ

±5V Electrical Characteristics

(A_V = +2, R_f = 750Ω, R_L = 100Ω, V_{CC} = ±5V, unless specified.

Symbol	**Parameter**	**Conditions**	**Typ**	**Min/Max Ratings** (Note 2)			**Units**
Ambient Temperature		CLC5602IN/IM	+25˚C	+25˚C	0 to 70˚C	−40 to 85˚C	
Frequency Domain Response							
	-3dB Bandwidth	V_O =1.0V_{PP}	135	115	105	100	MHz
		V_O =4.0V_{PP}	48	45	42	40	MHz
	−0.1dB Bandwidth	V_O =1.0V_{PP}	20	18	15	12	MHz
	Gain Peaking	<200MHz, V_O =1.0V_{PP}	0	0.5	0.9	1.0	dB
	Gain Rolloff	<30MHz, V_O=1.0V_{PP}	0.1	0.3	0.4	0.5	dB
	Linear Phase Deviation	<30MHz, V_O = 1.0V_{PP}	0.15	0.3	0.4	0.4	deg
	Differential Gain	NTSC, R_L = 150Ω	0.06	0.18	-	-	%
	Differential Phase	NTSC, R_L = 150Ω	0.02	0.04	-	-	deg
Time Domain Response							
	Rise and Fall Time	2V Step	5.7	6.2	6.8	7.3	ns
	Settling Time to 0.05%	2V Step	15	25	40	60	ns
	Overshoot	2V Step	18	20	22	22	%
	Slew Rate	2V Step	300	225	190	175	V/µs
Distortion And Noise Response							
	2nd Harmonic Distortion	2V_{PP}, 1MHz	−86	−82	−79	−79	dBc
		2V_{PP}, 1MHz; R_L=1KΩ	−87	−83	−80	−80	dBc
		2V_{PP}, 5MHz	−70	−64	−61	−60	dBc
	3rd Harmonic Distortion	2V_{PP}, 1MHz	−85	−81	−78	−78	dBc
		2V_{PP},1MHz; R_L = 1KΩ	−95	−90	−87	−87	dBc
		2V_{PP}, 5MHz	−66	−64	−61	−60	dBc
	Equivalent Input Noise						

±5V Electrical Characteristics (Continued)

(A_V = +2, R_f = 750Ω, R_L = 100Ω, V_{CC} = ±5V, unless specified.

Symbol	Parameter	Conditions	Typ	Min/Max Ratings (Note 2)			Units
Distortion And Noise Response							
	Voltage (e_{ni})	>1MHz	3.4	4.4	4.9	4.9	$nV/\sqrt{Hz}$
	Non-Inverting Current (i_{bn})	>1MHz	6.3	8.2	9.0	9.0	$pA/\sqrt{Hz}$
	Inverting Current (i_{in})	>1MHz	8.7	11.3	12.4	12.4	$pA/\sqrt{Hz}$
	Crosstalk (Input Referred)	10MHz, $1V_{PP}$	−72	-	-	-	dB
Static, DC Performance							
	Input Offset Voltage		2	6	7	8	mV
	Average Drift		8	-	-	-	µV/˚C
	Input Bias Current (Non-Inverting)		5	12	16	17	µA
	Average Drift		40	-	-	-	nA/˚C
	Input Bias Current (Inverting)		8	24	28	28	µA
	Average Drift		20	-	45	45	nA/˚C
	Power Supply Rejection Ratio	DC	48	45	43	43	dB
	Common Mode Rejection Ratio	DC	51	49	47	47	dB
	Supply Current (Per Channel)	$R_L = \infty$	1.6	1.9	2.0	2.0	mA
Miscellaneous Performance							
	Input Resistance (Non-Inverting)		0.59	0.47	0.43	0.43	MΩ
	Input Capacitance (Non-Inverting)		1.45	2.15	2.15	2.15	pF
	Common Mode Input Range		±4.2	±4.1	±4.1	±4.0	V
	Output Voltage Range	R_L = 100Ω	±3.8	±3.6	±3.6	±3.5	V
	Output Voltage Range	$R_L = \infty$	±4.0	±3.8	±3.8	±3.7	V
	Output Current		130	100	80	50	mA
	Output Resistance, Closed Loop	DC	40	70	70	90	mΩ

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

Note 2: Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

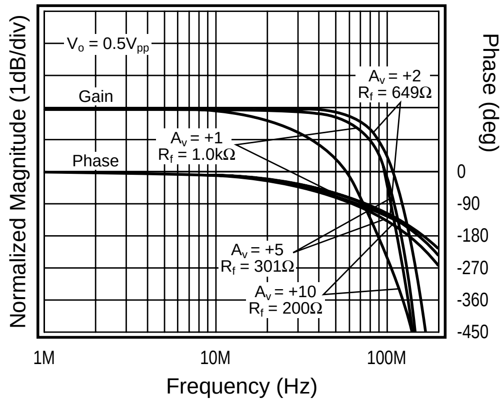
Note 3: AJ-level: spec. is 100% tested at +25˚C.

Note 4: The short circuit current can exceed the maximum safe output current

Note 5: $V_S = V_{CC} - V_{EE}$

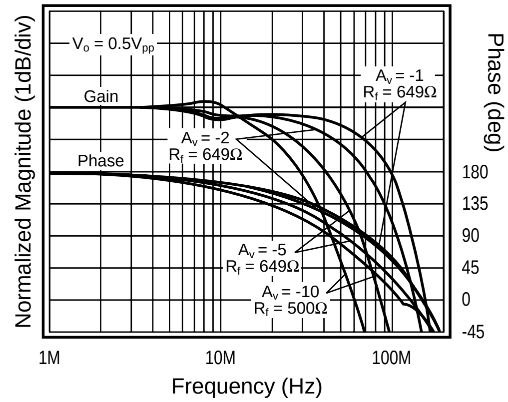
Typical Performance Characteristics (A_V = +2, R_f = 750Ω, R_L = 100Ω, V_S = +5V[1], V_CM = V_{EE} + (V_S/2), R_L tied to V_{CM}, unless specified)

Non-Inverting Frequency Response



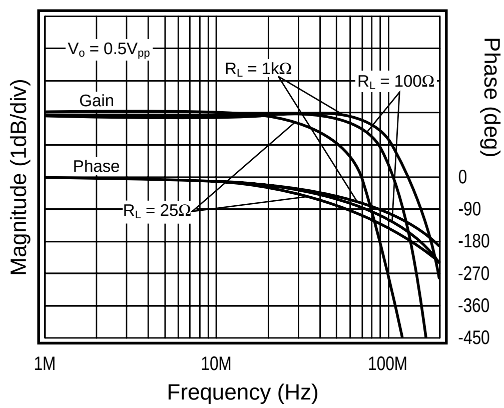
DS015000-4

Inverting Frequency Response



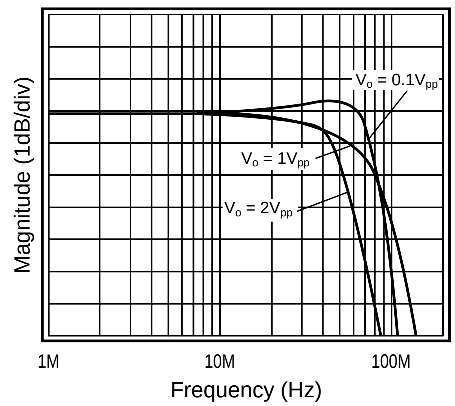
DS015000-5

Frequency Response vs. R_L



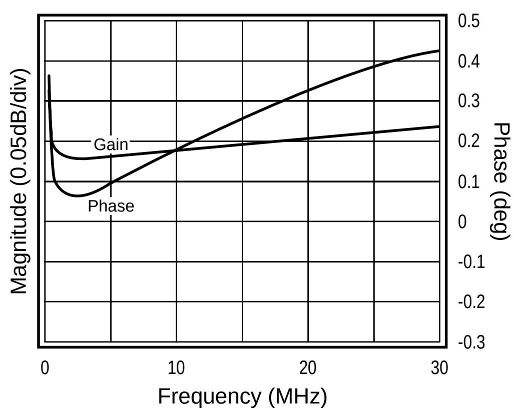
DS015000-6

Frequency Response vs. V_O



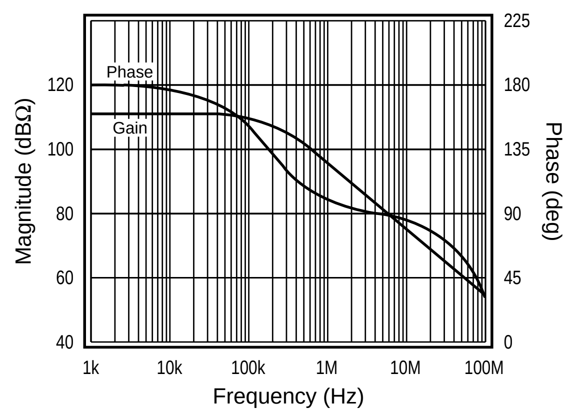
DS015000-7

Gain Flatness & Linear Phase



DS015000-8

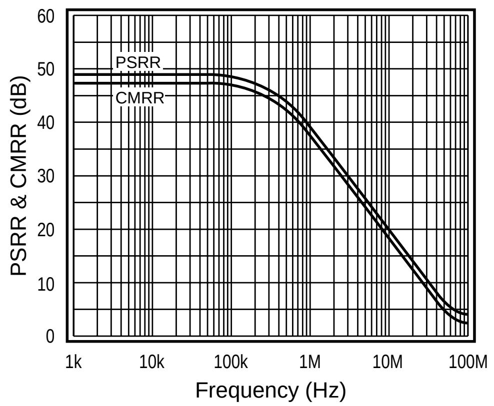
Open Loop Transimpedance Gain Z(s)



DS015000-9

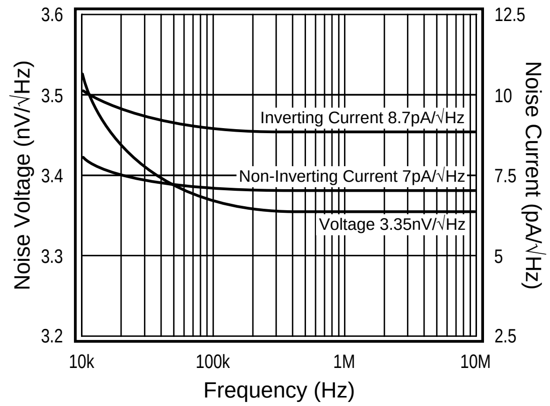
Typical Performance Characteristics (A_V = +2, R_f = 750Ω, R_L = 100Ω, V_S = +5V[1], V_CM = V_{EE} + (V_S/2), R_L tied to V_{CM}, unless specified) (Continued)

PSRR & CMRR



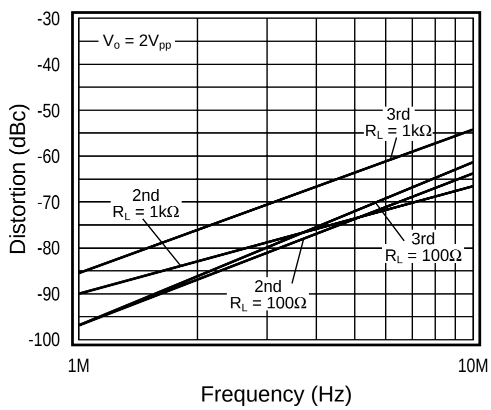
DS015000-10

Equivalent Input Noise



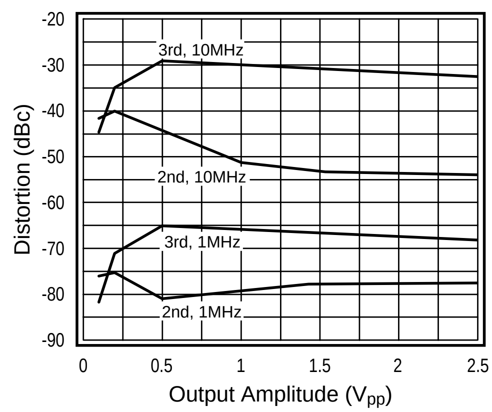
DS015000-11

2nd & 3rd Harmonic Distortion



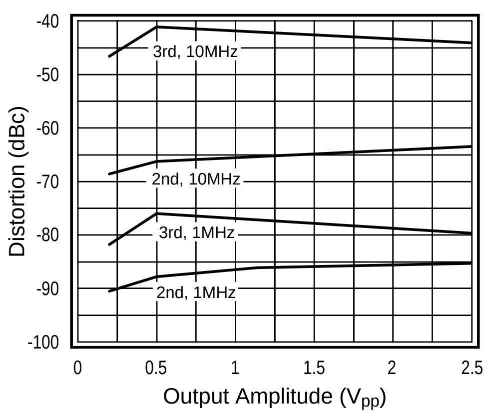
DS015000-12

2nd & 3rd Harmonic Distortion, R_L=25Ω



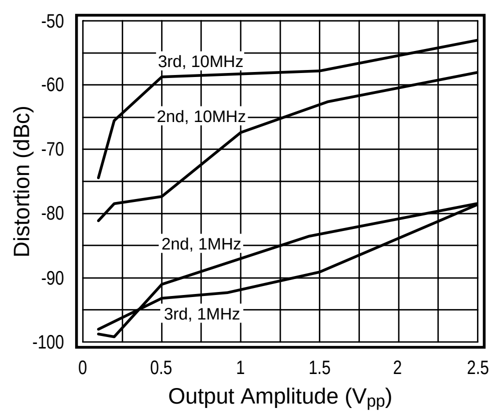
DS015000-13

2nd & 3rd Harmonic Distortion, R_L=100Ω



DS015000-14

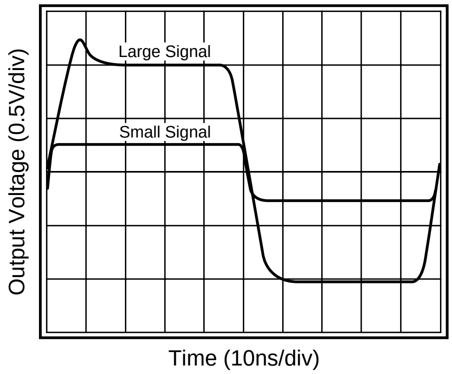
2nd & 3rd Harmonic Distortion, R_L=1kΩ



DS015000-15

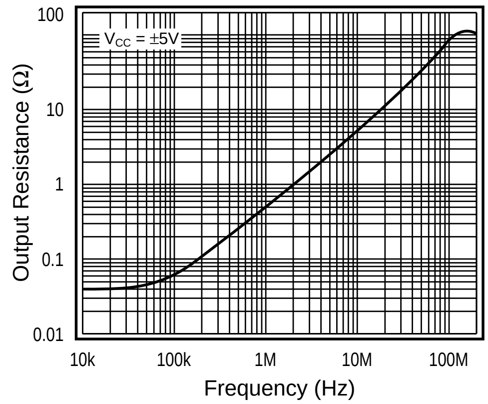
Typical Performance Characteristics (A_V = +2, R_f = 750Ω, R_L = 100Ω, V_S = +5V[1], V_CM = V_{EE} + (V_S/2), R_L tied to V_{CM}, unless specified) (Continued)

Large & Small Signal Pulse Response



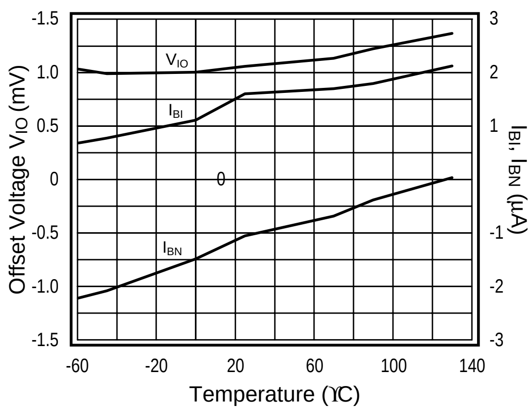
DS015000-16

Closed Loop Output Resistance



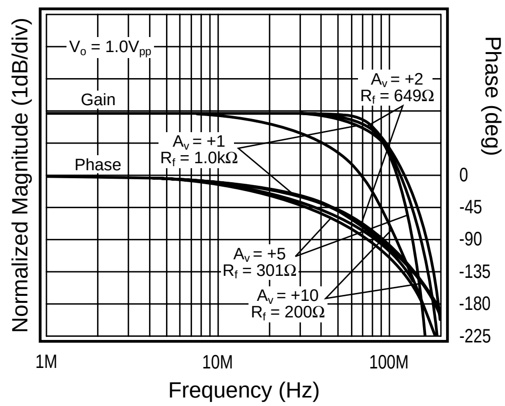
DS015000-17

I_{BI}, I_{BN}, V_{IO} vs. Temperature



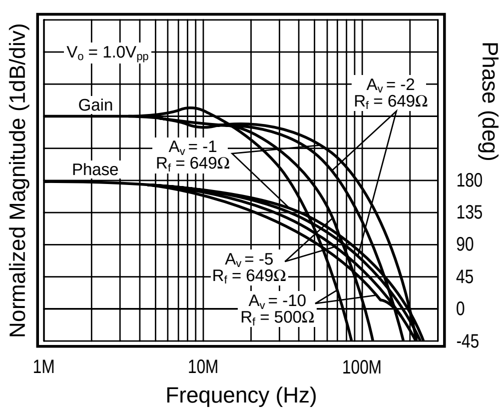
DS015000-18

Frequency Response



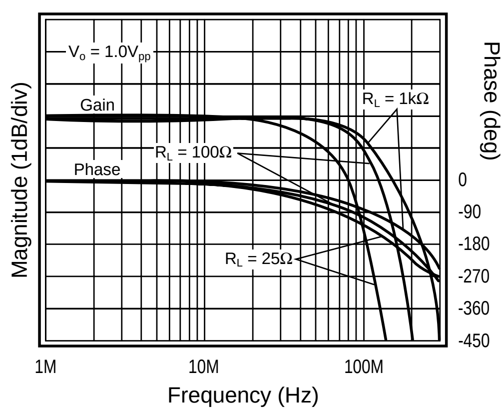
DS015000-19

Inverting Frequency Response



DS015000-20

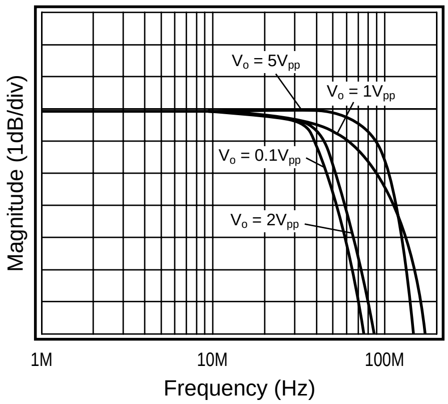
Frequency Response vs. R_L



DS015000-21

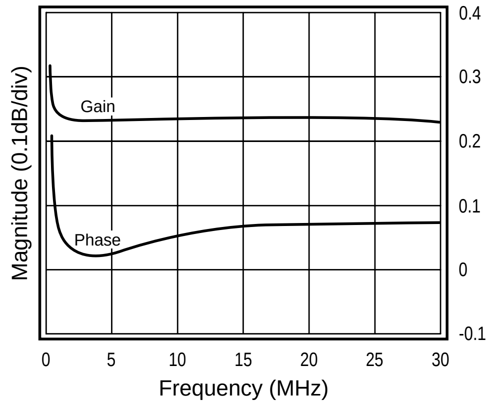
Typical Performance Characteristics (A_V = +2, R_f = 750Ω, R_L = 100Ω, V_S = +5V[1], V_CM = V_{EE} + (V_S/2), R_L tied to V_{CM}, unless specified) (Continued)

Frequency Response vs. V_O



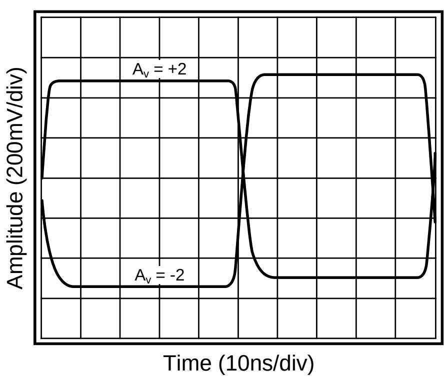
DS015000-22

Gain Flatness & Linear Phase



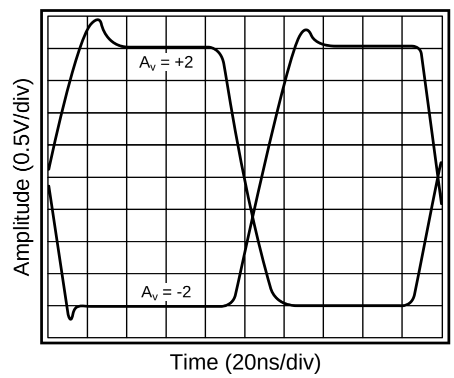
DS015000-23

Small Signal Pulse Response



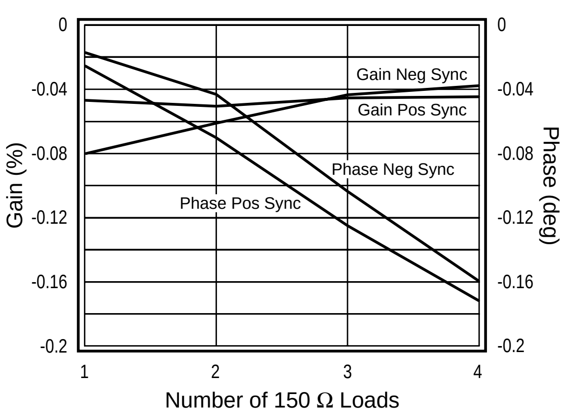
DS015000-24

Large Signal Pulse Response



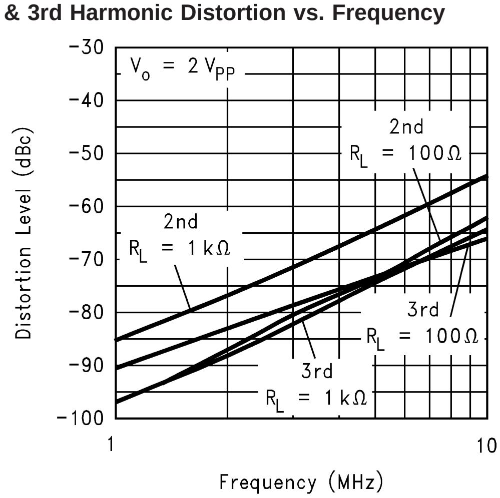
DS015000-25

Differential Gain and Phase



DS015000-26

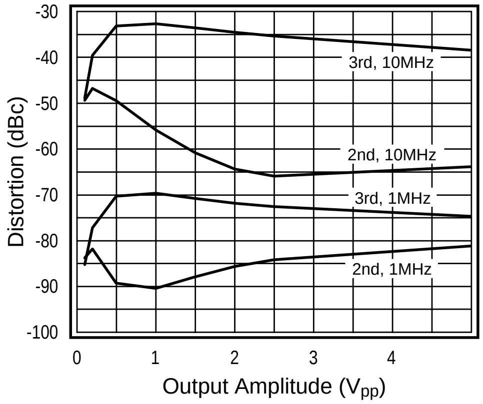
2nd & 3rd Harmonic Distortion vs. Frequency



DS015000-27

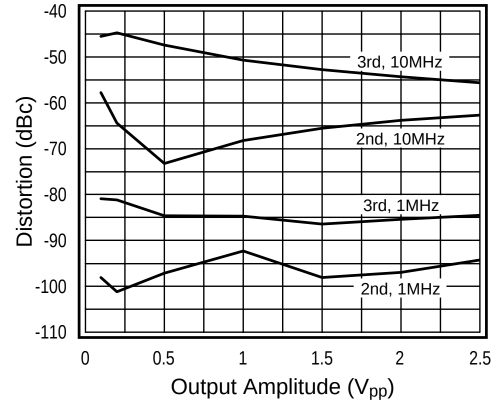
Typical Performance Characteristics (A_V = +2, R_f = 750Ω, R_L = 100Ω, V_S = +5V[1], V_CM = V_{EE} + (V_S/2), R_L tied to V_{CM}, unless specified) (Continued)

2nd & 3rd Harmonic Distortion, R_L=25Ω



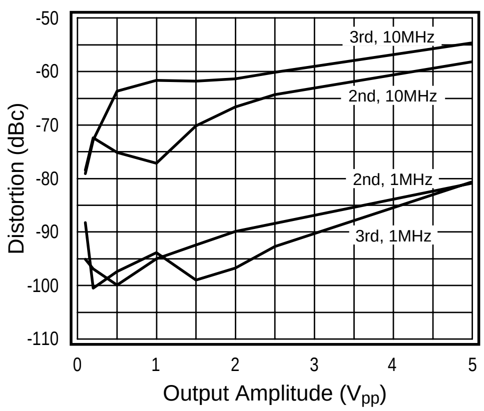
DS015000-28

2nd & 3rd Harmonic Distortion, R_L=100Ω



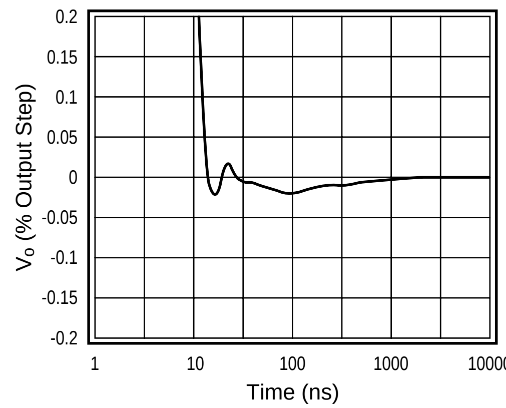
DS015000-29

2nd & 3rd Harmonic Distortion, R_L=1kΩ



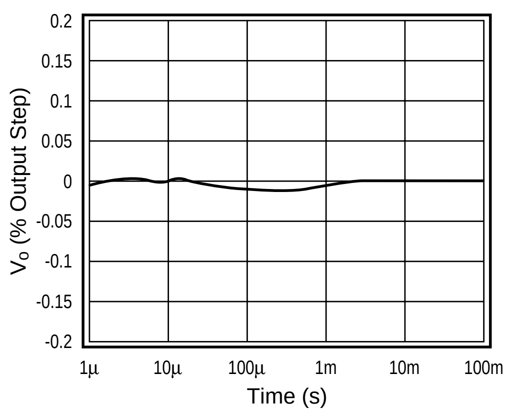
DS015000-30

Short Term Settling Time



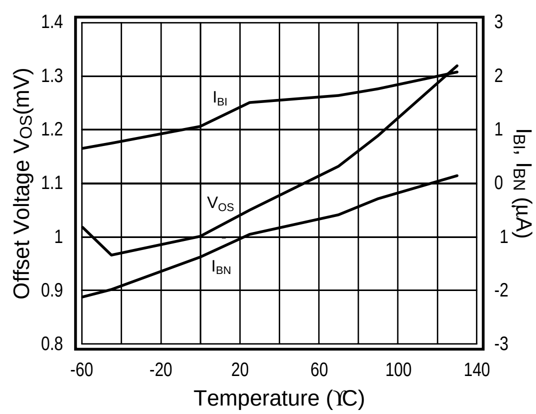
DS015000-31

Long Term Settling Time



DS015000-32

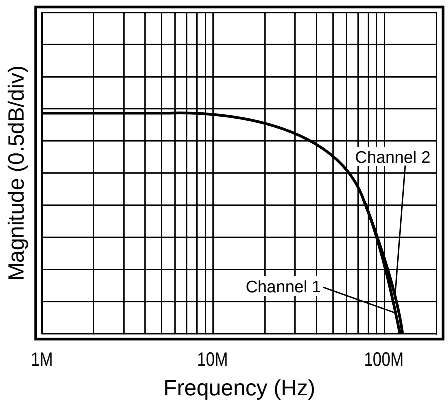
I_{BI}, I_{BN}, V_{os} vs. Temperature



DS015000-33

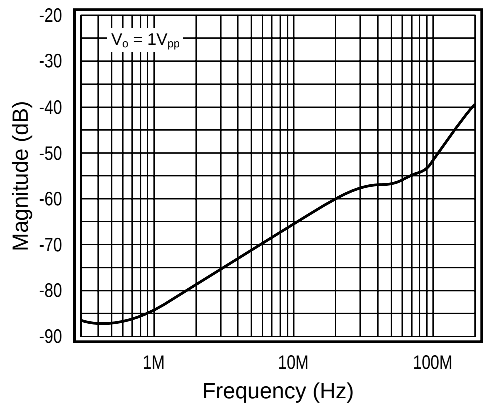
Typical Performance Characteristics (A_V = +2, R_f = 750Ω, R_L = 100Ω, V_S = +5V[1], V_CM = V_{EE} + (V_S/2), R_L tied to V_{CM}, unless specified) (Continued)

Channel Matching



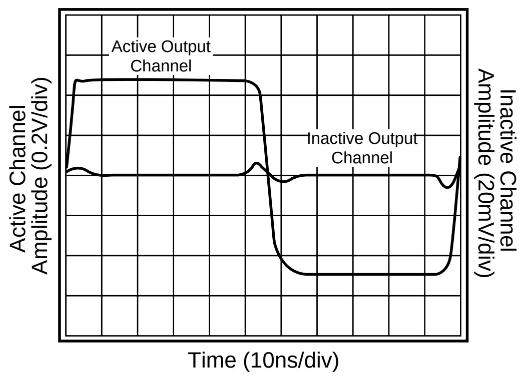
DS015000-34

Input Referred Crosstalk



DS015000-35

Pulse Crosstalk



DS015000-36

Application Division

The CLC5602 is a current feedback amplifier fabricated in an advanced complementary bipolar process. The CLC5602 operates from a single 5V supply or dual ±5V supplies. Operating from a single supply, the CLC5602 has the following features:

- Provides 100mA of output current while consuming 7.5mW of power
- Offers low −80/−82dB 2nd and 3rd harmonic distortion
- Provides BW60MHz and 1MHz distortion <−65dBc at V_O = 2.0V_{PP}

The CLC5602 performance is further enhanced in ±5V supply applications as indicated in the **±5V Electrical Characteristics** table and **±5V Typical Performance** plots.

Current Feedback Amplifiers

Some of the key features of current feedback technology are:

- Independence of AC bandwidth and voltage gain
- Inherently stable at unity gain
- Adjustable frequency response with feedback resistor
- High slew rate
- Fast settling

Current feedback operation can be described using a simple equation. The voltage gain for a non-inverting or inverting current feedback amplifier is approximately by Equation 1.

$$\frac{V_o}{V_{in}} = \frac{A_V}{1+\frac{R_f}{Z(j\omega)}} \quad (1)$$

where:

- A_V is the closed loop DC voltage gain
- R_f is the feedback resistor
- $Z(j\omega)$ is the CLC5602's open loop transimpedance gain
- $Z(j\omega)/R_f$ is the loop gain

The denominator of Equation 1 is approximately equal to 1 at low frequencies. Near the −3dB corner frequency, the interaction between R_f and $Z(j\omega)$ dominates the circuit performance. The value of the feedback resistor has a large affect on the circuits performance. Increasing R_f has the following affects:

- Decreases loop gain
- Decreases bandwidth
- Reduces gain peaking

Application Division (Continued)

- Lowers pulse response overshoot
- Affects frequency response phase linearity

Refer to the **Feedback Resistor Selection** section for more details on selecting a feedback resistor value.

CLC5602 Design Information

Single Supply Operation (V_{CC}=+5V, V_{EE}=GND) The specifications given in the +5V Electrical Characteristics table for single supply operation are measured with a common mode voltage (V_{cm}) of 2.5V. V_{cm} is the voltage around which the inputs are applied and the output voltages are specified.

Operating from a single +5V supply, the Common Mode Input Range (CMIR) of the CLC5602 is typically +0.8V to +4.2V. The typical output range with R_L=100Ω is +1.0V to +4.0V.

For single supply DC coupled operation, keep input signal levels above 0.8V DC. For input signals that drop below 0.8V DC, AC coupling and level shifting the signal are recommended. The non-inverting and inverting configurations for both input conditions are illustrated in the following 2 sections.

DC Coupled Single Supply Operation*Figure 1* and *Figure 2* show the recommended non-inverting and inverting configurations for input signals that remain above 0.8V DC.

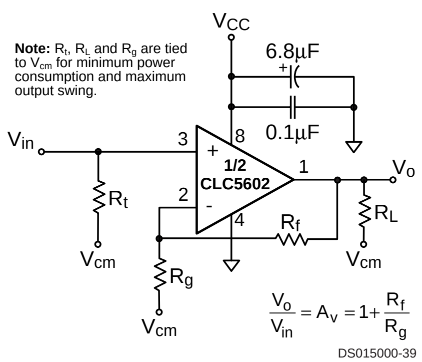


FIGURE 1. Non-Inverting Configuration

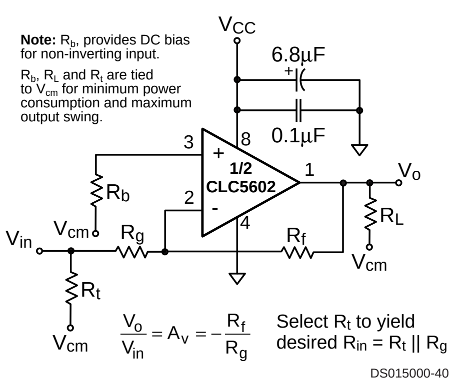


FIGURE 2. Inverting Configuration

AC Coupled Single Supply Operation

Figure 3 and *Figure 4* show possible non-inverting and inverting configurations for input signals that go below 0.8V DC. The input is AC coupled to prevent the need for level shifting the input signal at the source. The resistive voltage divider biases the non-inverting input to V_{CC} ÷ 2 = 2.5V (For V_{CC} = +5V).

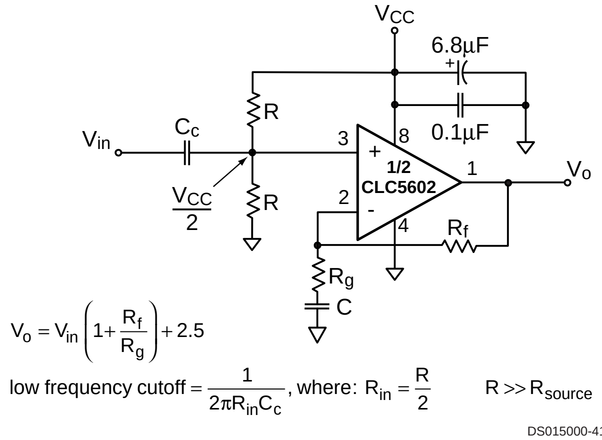


FIGURE 3. AC Coupled Non-Inverting Configuration

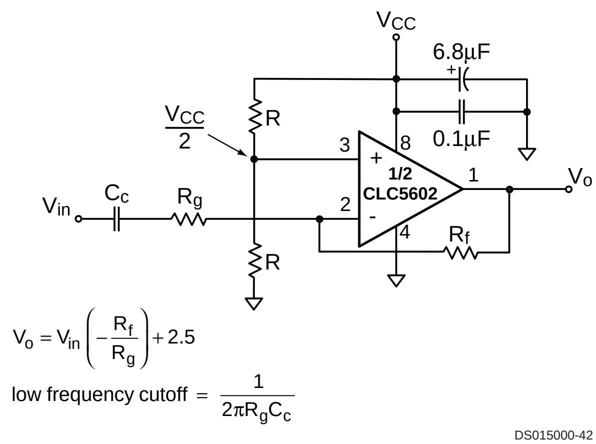


FIGURE 4. AC Coupled Inverting Configuration

Dual Supply Operation

The CLC5602 operates on dual supplies as well as single supplies. The non-inverting and inverting configurations are shown in *Figure 5* and *Figure 6*.

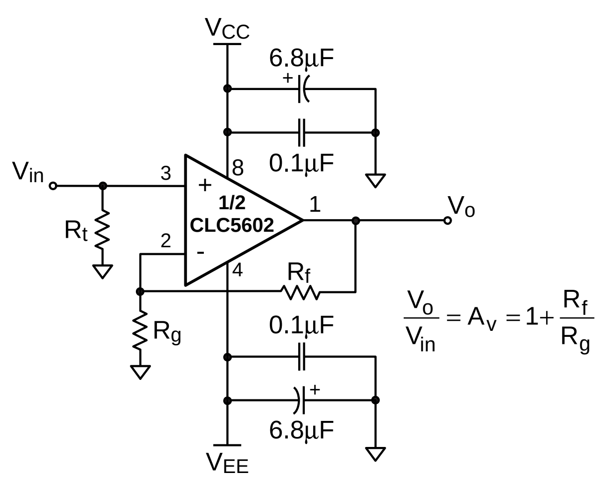


FIGURE 5. Dual Supply Non-Inverting Configuration

Application Division (Continued)

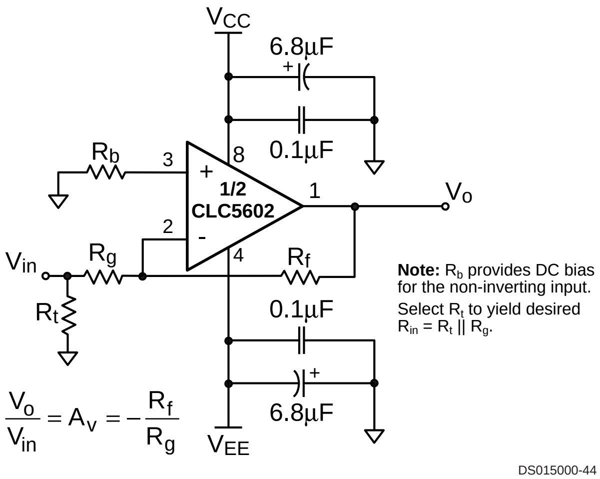


FIGURE 6. Dual Supply Inverting Configuration

Feedback Resistor Selection

The feedback resistor, R_f, affects the loop gain and frequency response of a current feedback amplifier. Optimum performance of the CLC5602, at a gain of +2V/V, is achieved with R_f equal to 750Ω. The frequency response plots in the Typical Performance sections illustrate the recommended R_f for several gains. These recommended values of R_f provide the maximum bandwidth with minimal peaking. Within limits, R_f can be adjusted to optimize the frequency response.

- Decrease R_f to peak frequency response and extend bandwidth
- Increase R_f to roll off frequency response and compress bandwidth

As a rule of thumb, if the recommended R_f is doubled, then the bandwidth will be cut in half.

Unity Gain Operation

The recommended R_f for unity gain (+1V/V) operation is 1kΩ. R_f is left open. Parasitic capacitance at the inverting node may require a slight increase in R_f to maintain a flat frequency response.

Load Termination

The CLC5602 can source and sink near equal amounts of current. For optimum performance, the load should be tied to V_{cm}.

Driving Cables and Capacitive Loads

When driving cables, double termination is used to prevent reflections. For capacitive load applications, a small series resistor at the output of the CLC5602 will improve stability and settling performance. The **Frequency Response vs. C_L** plot, shown below in *Figure 7*, gives the recommended series resistance value for optimum flatness at various capacitive loads.

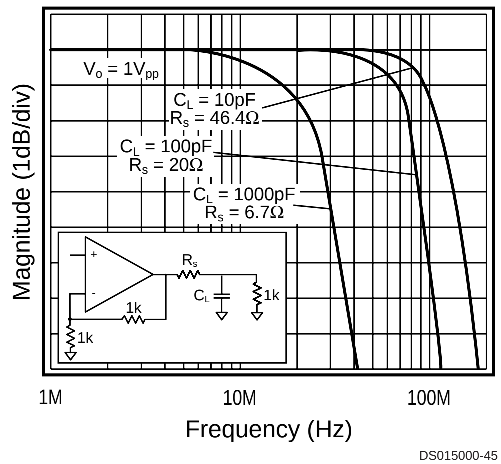


FIGURE 7. Frequency Response vs. C_L

Transmission Line Matching

One method for matching the characteristic impedance (z_o) of a transmission line or cable is to place the appropriate resistor at the input or output of the amplifier.

Figure 8 shows typical inverting and non-inverting circuit configurations for matching transmission lines.

Non-inverting gain applications:

- Connect R_3 directly to ground.
- Make R_1, R_2, R_6, and R_7 equal to Z_o.
- Use R_3 to isolate the amplifier from reactive loading caused by the transmission line, or by parasitics.

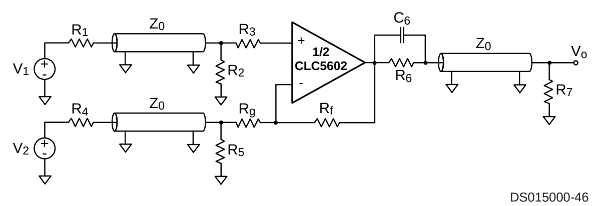


FIGURE 8. Transmission Line Matching

Inverting gain applications:

- Connect R_3 directly to ground.
- Make R_4, R_6, and R_7 equal to Z_o.
- Make R_5, II R_g= Z_o.

The input and output matching resistors attenuate the signal by a factor of 2, therefore additional gain is needed. Use C_6 to match the output transmission line over a greater frequency range. C_6 compensates for the increase of the amplifier's output impedance with frequency.

Power Dissipation

Follow these steps to determine the power consumption of the CLC5602:

1. Calculate the quiescent (no-load) power: $P_{amp}=1_{CC}\ (V_{CC}-V_{EE})$
2. Calculate the RMS power at the output stage: $P_o=(V_{CC}-V_{load})(I_{load})$, where V_{load} and I_{load} are the RMS voltage and current across the external load.
3. Calculate the total RMS power: $P_t=P_{amp}+P_o$

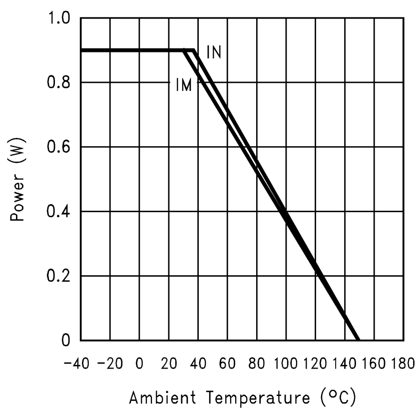
Application Division (Continued)

The maximum power that the DIP and SOIC packages can dissipate at a given temperature is illustrated in *Figure 9*. The power derating curve for any CLC5602 package can be derived by utilizing the following equation:

$$\frac{(150° - T_{amb})}{\theta_{JA}}$$

where T_{amb} = Ambient temperature (˚C)

θ_{JA}= Thermal resistance, from junction to ambient, for a given package (˚C/W)



DS015000-48

FIGURE 9. Power Derating Curves

Layout Considerations

A proper printed circuit layout is essential for achieving high frequency performance. National provides evaluation boards for the CLC5602 (CLC730038-DIP, CLC730036-SOIC) and suggests their use as a guide for high frequency layout and as an aid for device testing and characterization.

General layout and supply bypassing play major roles in high frequency performance. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF tantalum and 0.1µF ceramic capacitors on both supplies.
- Place the 6.8µF capacitors within 0.75 inches of the power pins.
- Place the 0.1µF capacitors less than 0.1 inches from the power pins.
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.
- Use flush-mount printed circuit board pins for prototyping, never use high profile DIP sockets.

Evaluation Board Information

A data sheet is available for the CLC730038/CLC730036 evaluation boards. The evaluation board data sheet provides:

- Evaluation board schematics
- Evaluation board layouts
- General information about the boards

The evaluation boards are designed to accommodate dual supplies. The boards can be modified to provide single supply operation. For best performance; 1) do not connect the unused supply, 2) ground the unused supply pin.

SPICE Models

SPICE models provide a means to evaluate amplifier designs. Free SPICE models are available for National's monolithic amplifiers that:

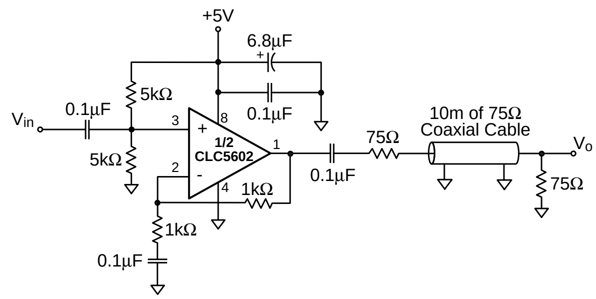
- Support Berkeley SPICE 2G and its many derivatives
- Reproduce typical DC, AC, Transient, and Noise performance
- Support room temperature simulations

The readme file that accompanies the diskette lists released models, and provides a list of modeled parameters. The application note OA-18, Simulation SPICE Models for National's Op Amps, contains schematics and a reproduction of the readme file.

Application Circuits

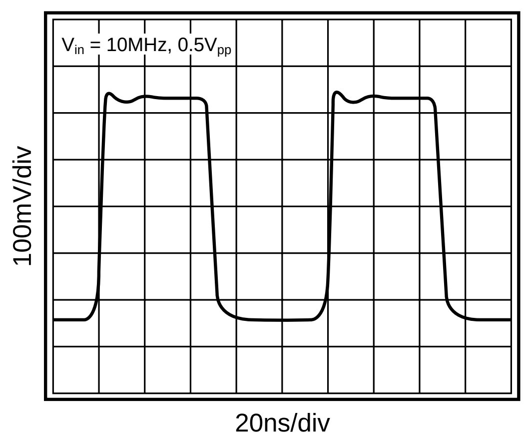
Single Supply Cable Driver

The typical application shown below shows one of the CLC5602 amplifiers driving 10m of 75Ω coaxial cable. The CLC5602 is set for a gain of +2V/V to compensate for the divide-by-two voltage drop at V_o.



DS015000-49

FIGURE 10. Single Supply Cable Driver



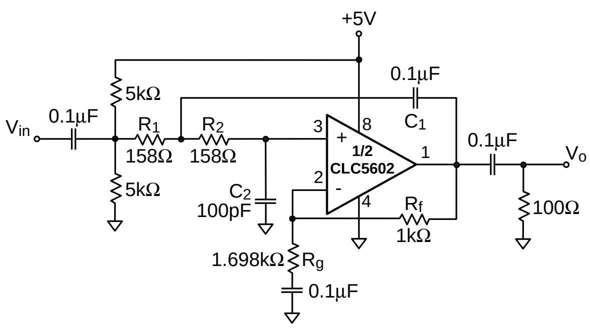
DS015000-50

FIGURE 11. Response After 10m of Cable

Single Supply Lowpass Filter

Figure 12 and *Figure 13* illustrate a lowpass filter and design equations. The circuit operates from a single supply of +5V. The voltage divider biases the non-inverting input to 2.5V. And the input is AC coupled to prevent the need for level shifting the input signal at the source. Use the design equations to determine R_1, R_2, C_1, and C_2 based on the desired Q and corner frequency.

Application Division (Continued)



DS015000-51

FIGURE 12. Lowpass Filter Topology

$$\text{Gain} = K = 1 + \frac{R_f}{R_g}$$

$$\text{Corner frequency} = \omega_c = \sqrt{\frac{1}{R_1 R_2 C_1 C_2}}$$

$$Q = \frac{1}{\sqrt{\frac{R_2C_2}{R_1C_1}} + \sqrt{\frac{R_1C_2}{R_2C_1}} + (1-K)\sqrt{\frac{R_1C_1}{R_2C_2}}}$$

$$\text{For } R_1 = R_2 = R \text{ and } C_1 = C_2 = C$$

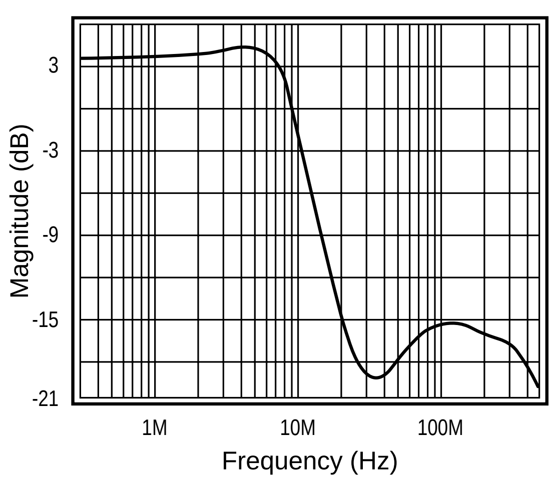
$$\omega_c = \frac{1}{RC}$$

$$Q = \frac{1}{(3-K)}$$

DS015000-52

FIGURE 13. Design Equations

This example illustrates a lowpass filter with Q = 0.707 and corner frequency f_c = 10MHz. A Q of 0.707 was chosen to achieve a maximally flat, Butterworth response. *Figure 14* indicates the filter response.

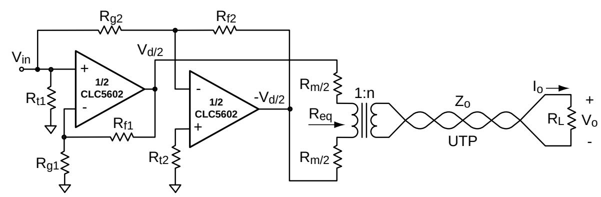


DS015000-53

FIGURE 14. Lowpass Response

Differential Line Driver with Load Impedance Conversion

The circuit shown in the **Typical Application** schematic on the front page and in *Figure 15*, operates as a differential line driver. The transformer converts the load impedance to a value that best matches the CLC5602's output capabilities. The single-ended input signal is converted to a differential signal by the CLC5602. The line's characteristic impedance is matched at both the input and the output. The schematic shows Unshielded Twisted Pair for the transmission line; other types of lines can also be driven.



DS015000-54

FIGURE 15. Differential Line Driver with Load Impedance Conversion

Set up the CLC5602 as a difference amplifier:

$$\frac{V_d}{V_{in}} = 2 \cdot \left(1 + \frac{R_{f1}}{R_{g1}}\right) = 2 \cdot \frac{R_{f2}}{R_{g2}}$$

Make the best use of the CLC5602's output drive capability as follows:

$$R_m + R_{eq} = \frac{2 \cdot V_{max}}{I_{max}}$$

where R_{eq} is the transformed value of the load impedance, V_{max} is the Output Voltage Range, and I_{max} is the maximum Output Current.

Match the line's characteristic impedance:

$$R_L = Z_o$$

$$R_m = R_{eq}$$

$$n = \sqrt{\frac{R_L}{R_{eq}}}$$

Select the transformer so that it loads the line with a value very near Z_o over frequency range. The output impedance of the CLC5602 also affects the match. With an ideal transformer we obtain:

$$\text{Return Loss} = -20 \cdot \log_{10} \left| \frac{n^2 \cdot Z_{o(5602)}(j\omega)}{Z_o} \right|, \text{dB}$$

where $Z_{O(5602)}(j\omega)$ is the output impedance of the CLC5602 and $|Z_{O(5602)}(j\omega)| << R_m$.

The load voltage and current will fall in the ranges:

Application Division (Continued)

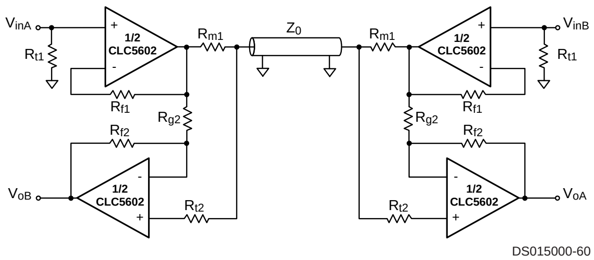
$$\left| V_o \right| \leq n \cdot V_{max}$$

$$\left| I_o \right| \leq \frac{I_{max}}{n}$$

The CLC5602's high output drive current and low distortion make it a good choice for the application.

Full Duplex Cable Driver

The circuit shown in Fig 16 below, operates as a full duplex cable driver which allows simultaneous transmission and reception of signals on one transmission line. The circuit on either side of the transmission line uses are CLC5602 as a cable driver, and the second CLC5602 as a receiver. V_{oA} is an attenuated version of Vi_{nA}, while V_{oB} is an attenuated of V_{inB}.



Full Duplex Cable Driver

R_{m1} is used to match the transmission line. R_{f2} and R_{g2} set the DC gain of the CLC5602, which is used in a difference mode. R_{t2} provides good CMRR and DC offset. The transmitting CLC5602's are shown in a unity gain configuration because they consume the least power of any gain, for a given load. For proper operation we need R_{f2} = R_{g2}.

The receiver output voltage are:

$$V_{outA(B)} \approx V_{inA(B)} \cdot A + \frac{V_{inB(A)}}{2} \cdot \left(1 - \frac{R_{f2}}{R_{g2}} + \frac{Z_{o(5602)}(j\omega)}{R_{m1}}\right)$$

where A is the attenuation of the cable, $Z_{O(5602)}(j\omega)$ is the output impedance of the CLC5602 (see the *Close-Loop Output Resistance* plot), and $|Z_{O(5602)}(j\omega)| << R_{m1}$.

We selected the component values as follows:

- R_{f1} = 1.0kΩ, the recommended value for the CLC5602 at unity gain
- R_{m1} = Z_O = 50Ω, the characteristic impedance of the transmission line
- R_{f2} = R_{g2} = 750Ω ≥ R_{m1}, the recommended value for the CLC5602 at A_V = 2

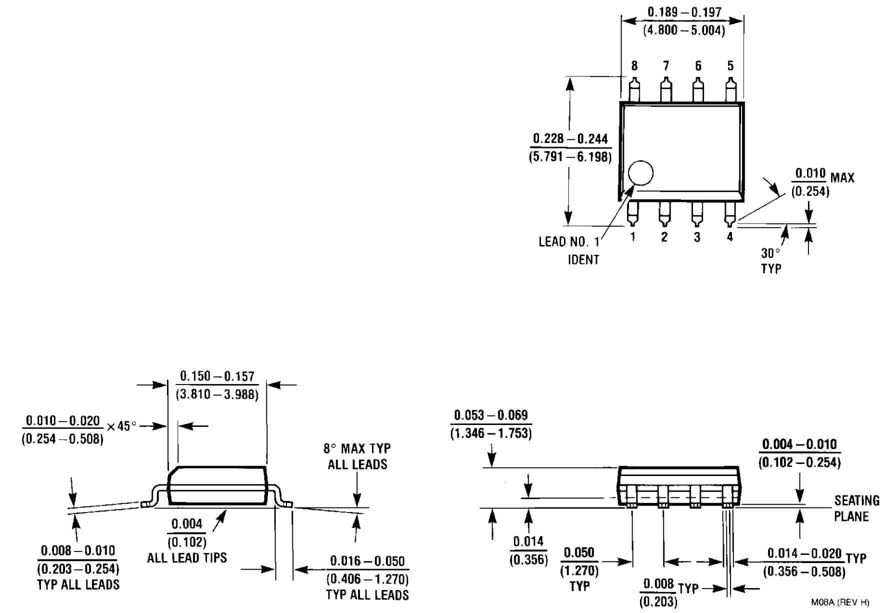
$$R_{t2} = (R_{f2} \| R_{g2}) \pm \frac{R_{m1}}{2} = 25\Omega$$

These values give excellent isolation from the other input:

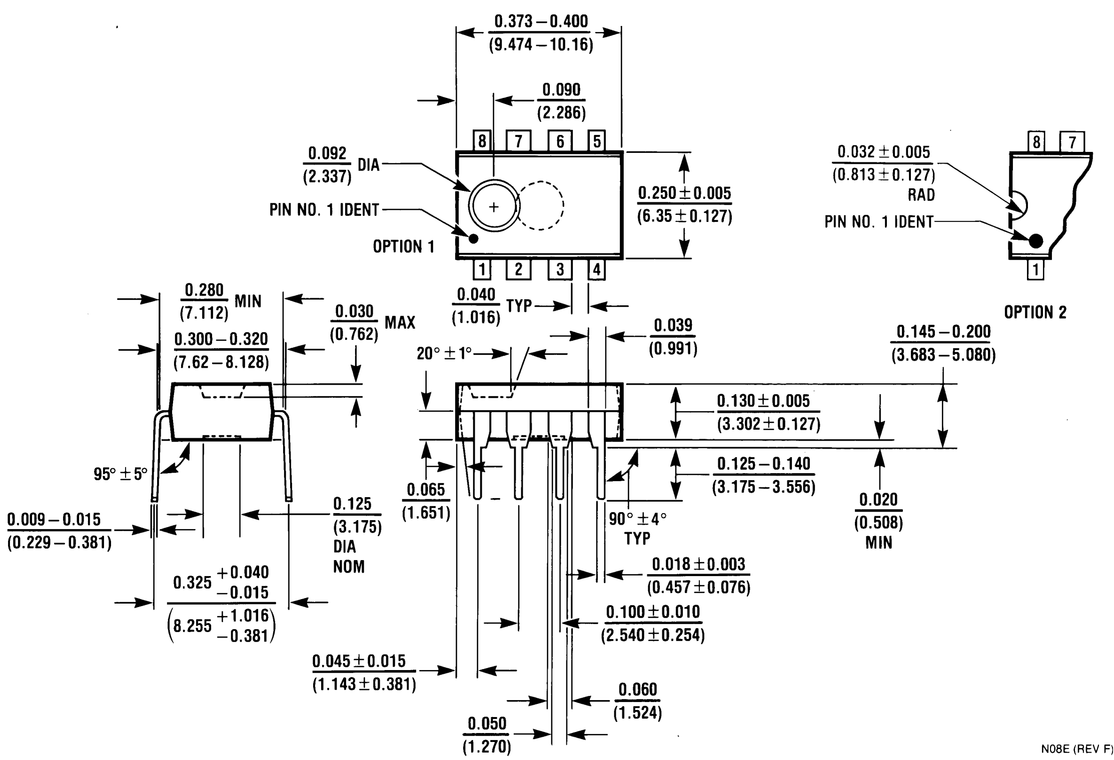
$$\frac{V_{oA(B)}}{V_{inB(A)}} \approx -38\text{dB},\ f = 5.0\text{MHz}$$

The CLC5602 provides large output current drive, while consuming little supply current, at the nominal bias point. It also produces low distortion with large signal swings and heavy loads. These features make the CLC5602 an excellent choice for driving transmission lines.

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin SOIC
NS Package Number M08A



8-Pin MDIP
NS Package Number N08E

Notes

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